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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,206	07/20/2001	Michael Beuten	10191/1873	2708

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EXAMINER	
RAMPURIA, SATISH	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,206	BEUTEN ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. This action is in response to the RCE received on August 29, 2006.
2. Claims amended by Applicant: 1, 10, and 13.
3. Claims 1-14 are pending.

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 29, 2006 has been entered.

Response to Arguments

5. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection (see the rejection below).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 7, 8, 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art in view of US Patent No. 6,502,209 to Bengtsson et al., hereinafter called Bengtsson in view of Japanese Patent No. JP405173890A to Weikmann hereinafter called Weikmann and further in view of US Patent No. 5,155,809 to Baker et al., hereinafter called Baker.

Per claims 1, 2, 3, 10, 13, and 14:

Admitted prior art discloses:

- A program stored in a computer readable medium, the program performing a method for monitoring an execution of a program that is executable on at least one microprocessor of a micro controller using a debug logic of the micro controller (Applicant's specification, page 2, lines 12-15 "The debug logic is used during the development of the program that is executable on the at least one microprocessor of the micro controller and is used for improvement of the visibility of the processes running in the micro controller")

- causing the debug logic to trigger an exception upon access to a specific address range during a program execution time (Applicant's specification, page 3, lines 1-2 "The debug logic can, as a rule, trigger an exception, e.g., an interrupt" and Applicant's specification, page 2, line 18 "The debug logic can learn from the address bus which selected address range was accessed")

- causing the debug logic to execute an exception routine after the exception is triggered during the program execution time (Applicant's specification, page 3, lines 23-25 "When access to one of these addresses is attempted, an exception is triggered and an exception routine is executed")

Admitted prior art does not explicitly disclose causing the at least one microprocessor to configure the debug logic.

However, Bengtsson discloses in an analogous computer system the debug chip is configured in DUT (device under test) (col. 4, lines 37-38 "debug chip 110C configured in DUT").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of configuring the microprocessor or DUT to debug logic as taught by Bengtsson in to the method of monitoring the program as taught in admitted prior art. The modification would be obvious because of one of ordinary skill in the art would be motivated configure the prior art microprocessor with debug logic to eliminate the excessive costs of the producing a special version chip for debugging purposes as suggested by Bengtsson (col. 2, lines 24-30).

Neither admitted prior art nor Bengtsson disclose the access to the specific address range includes illegal access to a storage area.

However, Weikmann discloses in an analogous computer system access to the specific address range includes illegal access to a storage area (page 8 [0032-0033, 0039] "address w which starts the secondary program in a storage region 34 is loaded to the auxiliary register 22. The value w is similarly memorized by the auxiliary register 24. When the address stored in said address register 14 is smaller than the address w stored in the auxiliary register 22, said comparator 21 outputs a signal (that is, when the secondary program has accessed the illegal storage locations from 0 to w-1). Moreover, it is equal to the value w with which the contents of

the program counter PC of a register file 13 are stored in the auxiliary register 24, or when it is more than it, a comparator 23 outputs a signal. In the case of the latter, the secondary program will be performed...").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method to access to the specific address range includes illegal access to a storage area as taught by Weikmann in to the method of monitoring the program as taught in combination system by admitted prior art and Bengtsson. The modification would be obvious because of one of ordinary skill in the art would be motivated to protect the access to an illegal storage area to provide the protection to the computer system as taught by Weikmann (page 6 [0009-0010]).

Neither admitted prior art nor Bengtsson disclose wherein the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, so as to provide a secure stack check without using the program execution time of the microprocessor.

However, Baker discloses in an analogous computer system wherein the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range ("Due to the multi -processing environment... all S/88 processor units in parallel" and "These handlers access the DMAC, BCU hardware, queues, linked lists, and all control parameters by presenting virtual addresses that lie within the address range of the `hidden` local store 210") and an exception routine is set up in reaction to a break point event in the stack, so as to provide a secure stack check without using the program execution time of the

microprocessor ("Each DMAC such as 209 has a single interrupt request (IRQ) output signal...").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method wherein the debug logic and its registers are operated in parallel to the program execution time to check a stack having the specific address range and an exception routine is set up in reaction to a break point event in the stack, so as to provide a secure stack check without using the program execution time of the microprocessor as taught by Baker in to the method of monitoring the program as taught in combination system by admitted prior art and Bengtsson. The modification would be obvious because of one of ordinary skill in the art would be motivated to run the program in parallel and have break point routine invoked at the specific address range to provide an improved method for CPU to interact with other data processing system as taught by Baker (col. 3, lines 30-56).

Per claim 4:

The rejection of claim 1 is incorporated, and further, admitted prior art does not explicitly disclose resetting the micro controller, starting up the micro controller again, and initializing the program.

However, Bengtsson discloses in an analogous computer system the power-on-reset unit coupled to the debug bus (col. 4, lines 21-24 "debug bus 140 is coupled to all chips... power-on-reset interrupts... other asynchronous events"). It is obvious to use the power-on-reset to reset microconroller and/or initialize the program.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the power-on-reset as taught by Bengtsson in to the method of monitoring the program as taught in admitted prior art. The modification would be obvious because of one of ordinary skill in the art would be motivated reset the microcontroller or DUT to make the new changes in effect.

Per claim 7 and 8:

The rejection of claim 1 is incorporated, and further, admitted prior art discloses:

- ***the debug logic monitors whether the program accesses a preselectable address range of a memory during the program execution time*** (Applicant's specification, page 2, lines 18-21 "The debug logic can learn from the address bus which selected address range was accessed, from the data bus, which data is to be written into the selected address range or was read out of the selected address range, and, from the control bus, whether a write or read access is to be performed on the selected address range")

Per claim 11:

The rejection of claim 10 is incorporated, and further, admitted prior art discloses:

- ***the control element corresponds to one of a read-only memory and a flash memory***

(Applicant's specification, page 2, lines 3-4 "internal control elements (e.g., a read-only memory or a flash memory), and/or further components")

Per claim 12:

The rejection of claim 10 is incorporated, and further, admitted prior art discloses:

- ***the micro controller is arranged in a motor vehicle*** (Applicant's specification, page 2, lines 4-5 "This type of micro controller is, for example, part of a controller for a motor vehicle")

7. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art, Bengtsson in view of US Patent No. 6,697,972 to Oshima et al., hereinafter called Oshima.

Per claims 5 and 6:

Neither admitted prior art nor Bengtsson discloses storing a fault in the memory and storing memory address.

However, Oshima discloses in an analogous computer system storing a fault in the memory and storing memory address (col. 5, lines 1-6 "OS fault detection time 13 and an OS fault recovery method 14 are stored with regard to a monitored subject ID 18 (address), and AP monitor fault detection time 15 and an AP monitor fault recovery method 16 are stored with regard to a monitored subject ID 20").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate storing a fault in the memory and storing memory address as taught by Oshima in corresponding to the combination system for monitoring the program as taught by admitted prior art and Bengtsson. The modification would be obvious because of one of ordinary skill in the art would be motivated to store fault type and memory address in the memory to start monitoring debugging where it left off as suggested by Oshima (col. 1, lines 40-46).

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over admitted prior art, Bengtsson in view of US Patent No. 6,535,811 to Rowland et al., hereinafter called Rowland.

Per claim 9:

Neither admitted prior art nor Bengtsson discloses a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory.

However, Rowland discloses in an analogous computer system a code sequence of the program, swapped out from a flash memory of the micro controller into a random access memory of the micro controller, in the flash memory (col. 5, lines 23-25 "memory holding the executable code, typically some type of ROM, had to be swapped with a memory having the new executable code "burned in."" and col. 5, lines 27-29 "flash memory 22 comprises a flash EPROM.. Thus, executable code for the microcontroller can be rewritten as necessary").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of swapping the code between memories as taught by Rowland into the method of monitoring the program as taught by the combination system of admitted prior art and Bengtsson. The modification would be obvious because of one of ordinary skill in the art would be motivated to swap the code between flash and RAM memories to read write the data control relationship during engine operation as suggested by (col. 2, lines 5-9).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 5:00 pm** Monday to Friday except every other Friday and federal holidays. Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: 571-272-2100**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Wei Y. Zhen** can be reached on **(571) 272-3708**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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